APPLICATION
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FOR: VOLTAGE GENERATING APPARATUS INCLUDING RAPID AMPLIFIER AND SLOW AMPLIFIER

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VOLTAGE GENERATING APPARATUS
INCLUDING RAPID AMPLIFIER AND SLOW AMPLIFIER

DESCRIPTION OF THE INVENTION
5   Field of the Invention

The present invention relates to a voltage generating apparatus for driving a capacitive load, and for example, to a gradation voltage generating apparatus used in an apparatus for driving a liquid crystal display (LCD) panel.

10   Description of the Related Art

Generally, an apparatus for driving an LCD panel is constructed by a gradation voltage generating circuit as a power supply voltage generating circuit for generating gradation voltages and decoders for selecting two of the gradation voltages and applying the two gradation voltages to the LCD panel.

In a first prior art LCD driving apparatus (see: Fig. 5 of JP-A-2000-20147), a gradation voltage generating circuit is constructed by a series of resistors and voltage-follower-type amplifiers for performing impedance transformation upon voltages at nodes of the resistors, and capacitors each connected to the voltage-follower-type amplifiers. Each of the voltage-follower-type amplifiers is a slow discharging amplifier or a slow charging amplifier with a single end type output circuit. This will be explained later in detail.

In the above-described first prior art LCD driving apparatus, however, since the transient response is very low due to the single end type output circuit, the above-mentioned capacitors are externally provided to suppress the fluctuation of the transient response. This results in increasing the apparatus in size and cost.

In a second prior art LCD driving apparatus (see:

Fig. 3 of JP-A-10-232383 and Fig. 7 of JP-A-2000-20147), a gradation voltage generating circuit is constructed by push-pull type amplifiers each including a slow discharging amplifier with a single end output circuit and a slow charging

5 amplifier with a single end output circuit instead of the voltage-follower-type amplifiers of the first prior art LCD driving apparatus each with a single end output circuit. This also will be explained later in detail.

In the above-described second prior art LCD driving

10 apparatus, however, since each of the discharging and charging amplifiers forming one push-pull type amplifier is of a slow type, the transient response is still low, which would invite flicker.

15 SUMMARY OF THE INVENTION

It is an object of the present invention to provide a voltage generating apparatus such as a gradation voltage generating circuit in an LCD driving apparatus having rapid transient response characteristics.

20 According to the present invention, in a voltage generating apparatus, a slow or rapid discharging amplifier is connected between an input terminal and an output terminal, and a rapid or slow charging amplifier is connected between the input terminal and the output terminal. An offset voltage

25 generating element is connected between the input terminal and one of the slow or rapid discharging amplifier and the rapid or slow charging amplifier, so that an input voltage applied to the slow or rapid discharging amplifier is higher than an input voltage applied to the rapid or slow-charging amplifier.

30 Thus, the transient response speed can be increased due to the presence of the rapid discharging amplifier or the rapid charging amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description set forth below, as compared with the prior art, with reference to the accompanying

5 drawings, wherein:

Fig. 1 is a circuit diagram illustrating a first prior art LCD driving apparatus;

Fig. 2A is a circuit diagram of the slow discharging amplifier as the voltage-follower-type amplifier of Fig. 1;

10 Fig. 2B is a circuit diagram of the slow charging amplifier as the voltage-follower-type amplifier of Fig. 1;

Fig. 3 is a table for showing examples of the voltages at the common electrode and the segment element of Fig. 1;

Fig. 4 is a circuit diagram including the slow

15 discharging amplifier of Fig. 2A;

Fig. 5 is a graph showing the voltage-to-current characteristics of the slow discharging amplifier of Fig. 4;

Fig. 6 is a timing diagram for explaining the operation of the slow discharging amplifier of Fig. 4;

20 Fig. 7 is a circuit diagram including the slow charging amplifier of Fig. 2B;

Fig. 8 is a graph showing the voltage-to-current characteristics of the slow charging amplifier of Fig. 7;

Fig. 9 is timing diagram for explaining the operation of

25 the slow charging amplifier of Fig. 7;

Fig. 10 is a circuit diagram illustrating a second prior art LCD driving apparatus;

Fig. 11 is a circuit diagram of the push-pull type amplifier of Fig. 10;

30 Fig. 12 is a circuit diagram including the push-pull type amplifier of Fig. 11;

Fig. 13 is a graph showing the voltage-to-current characteristics of the push-pull type amplifier of Fig. 12;

Fig. 14 is a timing diagram for explaining the operation of the push-pull type amplifier of Fig. 12;

Fig. 15 is a circuit diagram illustrating a first embodiment of the LCD driving apparatus according to the
5   present invention;

Fig. 16 is a circuit diagram of the push-pull type amplifier of Fig. 15;

Fig. 17 is a circuit diagram including the push-pull type amplifier of Fig. 16;

10   Fig. 18 is a graph showing the voltage-to-current characteristics of the push-pull type amplifier of Fig. 17;

Fig. 19 is a timing diagram for explaining the operation of the push-pull type amplifier of Fig. 17;

Fig. 20 is a circuit diagram illustrating a second
15   embodiment of the LCD driving apparatus according to the present invention;

Fig. 21 is a circuit diagram of the push-pull type amplifier of Fig. 20;

Fig. 22 is a circuit diagram including the push-pull type
20   amplifier of Fig. 21;

Fig. 23 is a graph showing the voltage-to-current characteristics of the push-pull type amplifier of Fig. 22;

Fig. 24 is a timing diagram for explaining the operation of the push-pull type amplifier of Fig. 22;

25   Fig. 25 is a timing diagram showing for explaining a modification of the operation of the push-pull type amplifier of Fig. 15;

Fig. 26 is a circuit diagram illustrating a third embodiment of the LCD driving apparatus according to the
30   present invention;

Fig. 27 is a circuit diagram of the push-pull type amplifier of Fig. 26;

Fig. 28 is a circuit diagram including the push-pull type

amplifier of Fig. 27;

Fig. 29 is a graph showing the voltage-to-current characteristics of the push-pull type amplifier of Fig. 28;

Fig. 30 is a timing diagram for explaining the operation
5   of the push-pull type amplifier of Fig. 28;

Fig. 31 is a timing diagram showing for explaining a modification of the operation of the push-pull type amplifier of Fig. 24;

Fig. 32 is a circuit diagram illustrating a third
10 embodiment of the LCD driving apparatus according to the present invention;

Fig. 33 is a circuit diagram of the push-pull type amplifier of Fig. 32;

Fig. 34 is a circuit diagram including the push-pull type
15 amplifier of Fig. 33;

Fig. 35 is a graph showing the voltage-to-current characteristics of the push-pull type amplifier of Fig. 34;

Fig. 36 is a timing diagram for explaining the operation of the push-pull type amplifier of Fig. 34;

20   Fig. 37 is a circuit diagram illustrating a modification of the push-pull amplifier of Fig. 27;

Fig. 38 is a circuit diagram illustrating a modification of the push-pull amplifier of Fig. 33;

Fig. 39 is a timing diagram showing the control signal
25 and its inverted signal of Figs. 37 and 38;

Fig. 40 is a circuit diagram illustrating a modification of the push-pull amplifier of Fig. 28;

Fig. 41 is a circuit diagram illustrating a modification of the push-pull amplifier of Fig. 34; and
30   Fig. 42 is a timing diagram showing the control signals of Figs. 40 and 41.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the description of the preferred embodiments, prior art LCD driving apparatuses will be explained with reference to Figs. 1, 2A, 2B, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13 and 14.

5   In Fig. 1, which illustrates a first prior art LCD driving apparatus (see: Fig. 5 of JP-A-2000-20147), a gradation voltage generating circuit 101 generates gradation voltages VLCD, VLC1, VLC2, VLC3, VLC4 and GND, and transmits the gradation voltages to decoders 102 and 103. Note that the

10   gradation voltage VLCD is generally much higher than a power supply voltage V_{DD}. For example, the gradation voltage VLCD can be generated by using a DC/DC converter.

The decoder 102 selects one of the gradation voltages VLCD, VLC1, VLC4 and GND in accordance with a frame

15   polarity signal FRAM having a positive polarity FRAM+ and a negative polarity FRAM- and a vertical synchronization signal VSYNC, so that the selected gradation voltage is applied to a common electrode COM of a liquid crystal panel 104.

On the other hand, the decoder 103 selects one of

20   the gradation voltages VLCD, VLC1, VLC2, VLC3, VLC4 and GND in accordance with the frame signal FRAM and a corresponding gradation data DT, so that the selected gradation voltage is applied to a segment electrode SEG of the liquid crystal panel 104. Note that there are generally a plurality of segment

25   electrodes in the liquid crystal panel 104; however, in order to simplify the description, only one segment is illustrated.

The gradation voltage generating circuit 101 is constructed by a series of resistors R1, R2, R3, R4 and R5 serving as a voltage divider for dividing a voltage between

30   VLCD and GND, voltage-follower-type amplifiers 1011, 1012, 1013 and 1014 for impedance transformation connected to nodes N1, N2, N3 and N4, respectively, of the resistors R1, R2, R3, R4 and R5, and capacitors C1, C2, C3, C4 and C5.

Each of the voltage-follower-type amplifiers 1011, 1012, 1013 and 1014 is constructed by a slow discharging amplifier as illustrated in Fig. 2A or a slow charging amplifier as illustrated in Fig. 2B in accordance with the

5   driving method for the liquid crystal panel 104. For example, each of the voltage-follower-type amplifiers 1011 and 1013 is constructed by the slow discharging amplifier as illustrated in Fig. 2A, and each of the voltage-follower-type amplifiers 1012 and 1014 is constructed by, the slow charging amplifier

10 as illustrated in Fig. 2B.

In more detail, as illustrated in Fig. 2A, the slow discharging amplifier is constructed by a differential amplifier formed by a current source 201, P-channel MOS transistors 202 and 203, N-channel MOS transistors 204 and 205,

15 a single end output circuit formed by a current source 206 and an N-channel MOS transistor 207, and a capacitor 208. In this case, the voltage at the node N1(N3) is applied to the gate of the transistor 203. On the other hand, the voltage VLC1 (VLC3) is negatively fed back to the gate of the MOS transistor

20 202. Note that if the voltage VLC1 (VLC3) is fed back to the gate of the MOS transistor 202 without the capacitor 208, oscillation may occur. Since the capacitor 208 serves as a phase compensating element, the amplifier of Fig. 2A is of a slow type for avoiding the above-mentioned oscillation.

25   Similarly, as illustrated in Fig. 2B, the slow charging amplifier is constructed by a differential amplifier formed by a current source 211, N-channel MOS transistors 212 and 203, P-channel MOS transistors 214 and 215, a single end output circuit formed by a current source 216 and a P-channel

30 MOS transistor 217, and a capacitor 218. In this case, the voltage at the node N2 (N4) is applied to the gate of the transistor 213. On the other hand, the voltage VLC2 (VLC4) is negatively fed back to the gate of the MOS transistor 212. Note

that if the voltage VLC2 (VLC4) is fed back to the gate of the MOS transistor 202 without the capacitor 218, oscillation may occur. Since the capacitor 218 serves as a phase compensating element, the amplifier of Fig. 2B is of a slow type for avoiding

5 the above-mentioned oscillation.

Each of the voltage-follower-type amplifiers 1011, 1012, 1013 and 1014 has a single-end type output circuit, not a push-pull type output circuit, so that no large penetration current flows therethrough, since a current flowing through

10 the single-end type output circuit is limited by the current source 206 or 216.

In Fig. 3, which shows examples of the voltages at the common electrode COM and the segment element SEG of the liquid crystal panel 104, in a selected mode, although the

15 difference in voltage between the common electrode COM and the segment electrode SEG is the same (for example, VLCD - GND), its polarity is switched by the frame polarity signal FRAM (FRAM+, FRAM-). On the other hand, in a non-selected mode, although the difference in voltage between the common

20 electrode COM and the segment electrode SEG is the same (VMIN), its polarity is switched by the frame polarity signal FRAM (FRAM+, FRAM-). Thus, the deterioration of liquid crystal of the liquid crystal panel 104 can be suppressed.

The operation of the slow discharging amplifier of

25 Fig. 2A will be explained next with reference to Figs. 4 and 5. In Fig. 4, the slow discharging amplifier of Fig. 2A is connected by the decoder 102 to the liquid crystal panel 104 so that the voltage VCOM at the common electrode COM is VCOM = VIN while the voltage VSEG at the segment electrode SEG

30 receives a voltage VL or VH via the decoder 103. In this case, the voltage (VCOM - VIN)-to-current I characteristics of the slow discharging amplifier of Fig. 4 are shown in Fig. 5. In Fig. 5, if VCOM>VIN, the current I is relatively large due to

the turning-ON of the transistor 207. On the other hand, if VCOM $\leq$ VIN, the current I is limited by the current source 206 while the transistor 207 is turned OFF.

Next, the transient characteristics of the voltage
5   VCOM of Fig. 4 are explained with reference to Fig. 6.

First, at time t1, when the voltage VSEG is increased by the decoder 103 from VL to VH, the voltage VCOM is also increased by the capacitive coupling. In this case, the slow discharging amplifier is operated, i.e., the
10   transistor 207 is turned ON to increase the backward current I, so that the voltage VCOM slowly recovers its original level VIN with a time $\tau 1$. In this case, a small undershoot as indicated X1 is generated.

Next, at time t2, when the voltage VSEG is decreased
15   by the decoder 103 from VH to VL, the voltage VCOM is also decreased by the capacitive coupling. In this case, the slow discharging amplifier is operated, i.e., the transistor 207 is turned OFF, so that the voltage VCOM very slowly recovers its original level VIN with a time $\tau 2$ which depends the
20   current value of the current source 206. Since the current value of the current source 206 is limited, as shown in Fig. 6, the time $\tau 2$ is larger than the time $\tau 1$. Therefore, no substantial overshoot as indicated by X2 is generated.

The operation of the slow charging amplifier of Fig.
25   2B will be explained next with reference to Figs. 7 and 8. In Fig. 7, the slow charging amplifier of Fig. 2B is connected by the decoder 102 to the liquid crystal panel 104 so that the voltage VCOM at the common electrode COM is VCOM = VIN while the voltage VSEG at the segment electrode SEG receives a
30   voltage VL or VH via the decoder 103. In this case, the voltage (VCOM - VIN)-to-current I characteristics of the slow charging amplifier of Fig. 7 are shown in Fig. 8. In Fig. 8, if VCOM < VIN, the current I is relatively large due to the turning-ON

of the transistor 217. On the other hand, if VCOM ≧ VIN, the current I is limited by the current source 216 while the transistor 217 is turned OFF.

Next, the transient characteristics of the voltage VCOM of Fig. 7 are explained with reference to Fig. 9.

First, at time t1, when the voltage VSEG is increased by the decoder 103 from VL to VH, the voltage VCOM is also increased by the capacitive coupling. In this case, the slow charging amplifier is operated, i.e., the transistor 217 is turned OFF, so that the voltage VCOM very slowly recovers its original level VIN with a time $\tau 2'$ using the current source 216. In this case, no substantial undershoot as indicated by X2' is generated.

Next, at time t2, when the voltage VSEG is decreased by the decoder 103 from VH to VL, the voltage VCOM is also decreased by the capacitive coupling. In this case, the slow charging amplifier is operated, i.e., the transistor 217 is turned ON to increase the forward current I, so that the voltage VCOM slowly recovers its original level VIN with a time $\tau 1'$. IN this case, a small overshoot as indicated by X1' is generated.

The time $\tau 2'$ depends the current value of the current source 216. Since the current value of the current source 216 is limited, as shown in Fig. 9, the time $\tau 2'$ is larger than the time $\tau 1'$.

In order to suppress the fluctuation of the times $\tau 2$ and $\tau 2'$, the capacitors C0, C1, C2, C3 and C4 are externally provided in the LCD driving apparatus of Fig. 1, since each of the capacitors C0, C1, C2, C3 and C4 has a relatively large capacitance. In this case, however, the LCD driving apparatus of Fig. 1 is increased in size and cost.

In Fig. 10, which illustrates a second prior art LCD driving apparatus (see: Fig. 3 of JP-A-10-232383 and Fig. 7

of JP-A-2000-20147), the gradation voltage generating circuit 101 of Fig. 1 is replaced by a gradation voltage generating circuit 301.

In the gradation voltage generating circuit 301, resistors r1, r2, r3 and r4 for generating offset voltages are inserted in series with the resistors R1, R2, R3, R4 and R5 of Fig. 1. Also, the single-end-type voltage-follower-type amplifiers 1011, 1012, 1013 and 1014 of Fig. 1 are replaced by push-pull type amplifiers 3011, 3012, 3013 and 3014, respectively. Each of the push-pull type amplifiers 3011, 3012, 3013 and 3014 is constructed by a slow discharging amplifier such as 3011N and a slow charging amplifier 3011P as illustrated in Fig. 11. Note that the resistance values of the resistors r1, r2, r3 and r4 are smaller than those of the resistors R1, R2, R3, R4 and R5, and therefore, an offset voltage ΔV is generated between the nodes N1 and N1', between the nodes N2 and N2', between the nodes N3 and N3', and between the nodes N4 and N4'.

In Fig. 10, the externally-provided capacitors C0, C1, C2, C3 and C4 of Fig. 1 are not provided, which would decrease the LCD driving apparatus of Fig. 8 in size and cost.

In Fig. 11, the slow discharging amplifier such as 3011N has the same configuration as the slow discharging amplifier of Fig. 2A, and the slow charging amplifier such as 3011P has the same configuration as the slow charging amplifier of Fig. 2B. That is, the two single end type amplifiers are combined into a push-pull type amplifier.

The operation of the push-pull type amplifier of Fig. 11 will be explained next with reference to Figs. 12 and 13. In Fig. 12, the push-pull type amplifier of Fig. 11 is connected by the decoder 102 to the liquid crystal panel 104 so that the voltage VCOM at the common electrode COM is VCOM = VIN while the voltage VSEG at the segment electrode SEG

receives a voltage VL or VH via the decoder 103. In this case, the voltage (VCOM - VIN)-to-current I characteristics of the push-pull type amplifier of Fig. 12 are shown in Fig. 13. In Fig. 13, if VCOM > VIN, the current I is relatively large due to the turning-ON of the transistor 207 of Fig. 11. On the other hand, if VCOM < VIN - ΔV where ΔV is the offset voltage, the current I is relatively large due to the turning-ON of the transistor 217.

Next, the transient characteristics of the voltage VCOM of Fig. 12 are explained with reference to Fig. 14.

First, at time t1, when the voltage VSEG is increased by the decoder 103 from VL to VH, the voltage VCOM is also increased by the capacitive coupling. In this case, the slow discharging amplifier 3011N is operated, i.e., the transistor 207 is turned ON to increase the backward current I, so that the voltage VCOM slowly recovers its original level VIN with a time τ1. In this case, a small undershoot as indicated by X1 is generated.

Next, at time t2, when the voltage VSEG is decreased by the decoder 103 from VH to VL, the voltage VCOM is also decreased by the capacitive coupling. In this case, the slow charging 3011P amplifier is operated, i.e., the transistor 217 is turned ON to increase the forward current I, so that the voltage VCOM slowly recovers its original level VIN with a time τ1'. In this case, a small overshoot as indicated by X1' is generated.

Note that, in Fig. 14, if the offset voltage ΔV is very small, no consideration can be given to the offset voltage ΔV. However, the offset voltage ΔV is indispensable in order to prevent the transistors 207 and 217 from being simultaneously turned ON to create a short-circuited state where an ON-ON current flows.

In the LCD driving apparatus of Fig. 10, however,

the discharging amplifier and the charging amplifier forming one push-pull type amplifier are both of a slow type including the capacitors 208 and 218 of Fig. 11, so that the transient response as shown in Fig. 14 is still slow which would invite

5   flicker.

In Fig. 15, which illustrates a first embodiment of the LCD driving apparatus according to the present invention, the gradation voltage generating circuit 301 of Fig. 10 is replaced by a gradation voltage generating circuit 1.

10   In the gradation voltage generating circuit 1, the push-pull type amplifiers 3011, 3012, 3013 and 3014 of Fig. 10 are replaced by push-pull type amplifiers 11, 12, 13 and 14, respectively. Each of the push-pull type amplifiers 11, 12, 13 and 14 is constructed by a slow discharging amplifier

15   such as 11N and a rapid charging amplifier 11p as illustrated in Fig. 16. Note that a resistor r is used for suppressing an ON-ON current when the transistors 207 and 217 or Fig. 16 are both turned ON.

In Fig. 16, the slow discharging amplifier such as

20   11N has the same configuration as the slow discharging amplifier of Fig. 11, and the rapid charging amplifier such as 11P has the same configuration as the slow charging amplifier of Fig. 11 except that the capacitor 218 is not provided.

25   The operation of the push-pull type amplifier of Fig. 16 will be explained next with reference to Figs. 17 and 18. In Fig. 17, the push-pull type amplifier of Fig. 16 is connected by the decoder 102 to the liquid crystal panel 104 so that the voltage VCOM at the common electrode COM is VCOM

30   = VIN while the voltage VSEG at the segment electrode SEG receives a voltage VL or VH via the decoder 103. In this case, the voltage (VCOM - VIN)-to-current I characteristics of the push-pull type amplifier of Fig. 17 are shown in Fig. 18. In

Fig. 13, if VCOM > VIN, the current I is relatively large due to the turning-ON of the transistor 207 of Fig. 16. On the other hand, if VCOM < VIN - ΔV where ΔV is the offset voltage, the current I is very large due to the turning-ON of the transistor

5 217, since the capacitor 218 is not provided.

Note that the rapid charging amplifier 11p may easily oscillate; in this case, however, since the rapid charging amplifier 11p is connected to the slow discharging amplifier 11N which may hardly oscillate, the rapid charging

10 amplifier 11p hardly oscillates.

Next, the transient characteristics of the voltage VCOM of Fig. 17 are explained with reference to Fig. 19.

First, at time t1, when the voltage VSEG is increased by the decoder 103 from VL to VH, the voltage VCOM

15 is also increased by the capacitive coupling. In this case, the slow discharging amplifier 11N is operated, i.e., the transistor 207 is turned ON to increase the backward current I, so that the voltage VCOM slowly recovers its original level VIN with a time τ1. In this case, a small undershoot as

20 indicated by X1 is generated.

Next, at time t2, when the voltage VSEG is decreased by the decoder 103 from VH to VL, the voltage VCOM is also decreased by the capacitive coupling. In this case, the rapid charging amplifier 11p is operated, i.e., the transistor 217

25 is turned ON to increase the forward current I, so that the voltage VCOM rapidly recovers its original level VIN with a time τ0'. In this case, a large overshoot may be generated; however, no substantial overshoot as indicated by X0' is generated due to the presence of the offset voltage ΔV.

30 Thus, in the LCD driving apparatus of Fig. 15, the charging amplifier forming one push-pull type amplifier is of a rapid type, the transient response as shown in Fig. 19 is rapid which would invite no flicker.

In Fig. 20, which illustrates a second embodiment of the LCD driving apparatus according to the present invention, the gradation voltage generating circuit 301 of Fig. 10 is replaced by a gradation voltage generating circuit 2.

5   In the gradation voltage generating circuit 2, the push-pull type amplifiers 3011, 3012, 3013 and 3014 of Fig. 10 are replaced by push-pull type amplifiers 21, 22, 23 and 24, respectively. Each of the push-pull type amplifiers 21, 22, 23 and 24 is constructed by a rapid discharging amplifier

10   such as 21n and a slow charging amplifier 21P as illustrated in Fig. 21. Note that a resistor r is used for suppressing an ON-ON current when the transistors 207 and 217 or Fig. 21 are both turned ON.

In Fig. 21, the rapid discharging amplifier such as

15   21n has the same configuration as the slow discharging amplifier of Fig. 11 except that the capacitor 208 is not provided, and the slow charging amplifier such as 21P has the same configuration as the slow charging amplifier of Fig. 11.

The operation of the push-pull type amplifier of Fig.

20   21 will be explained next with reference to Figs. 22 and 23. In Fig. 22, the push-pull type amplifier of Fig. 21 is connected by the decoder 102 to the liquid crystal panel 104 so that the voltage VCOM at the common electrode COM is VCOM = VIN while the voltage VSEG at the segment electrode SEG

25   receives a voltage VL or VH via the decoder 103. In this case, the voltage (VCOM - VIN)-to-current I characteristics of the push-pull type amplifier of Fig. 22 are shown in Fig. 23. In Fig. 23, if VCOM > VIN, the current I is very large due to the turning-ON of the transistor 207 of Fig. 21, since the

30   capacitor 208 is not provided. On the other hand, if VCOM < VIN - ΔV where ΔV is the offset voltage, the current I is relatively large due to the turning-ON of the transistor 217.

Note that the rapid discharging amplifier 21n may

easily oscillate; in this case, however, since the rapid discharging amplifier 21n is connected to the slow charging amplifier 21P which may hardly oscillate, the rapid discharging amplifier 21n hardly oscillates.

Next, the transient characteristics of the voltage VCOM of Fig. 22 are explained with reference to Fig. 24.

First, at time t1, when the voltage VSEG is increased by the decoder 103 from VL to VH, the voltage VCOM is also increased by the capacitive coupling. In this case, the rapid discharging amplifier 21n is operated, i.e., the transistor 207 is turned ON to increase the backward current I, so that the voltage VCOM rapidly recovers its original level VIN with a time $\tau 0$ $(< \tau 1)$. In this case, a large undershoot as indicated by X0 is generated.

Next, at time t2, when the voltage VSEG is decreased by the decoder 103 from VH to VL, the voltage VCOM is also decreased by the capacitive coupling. In this case, the slow charging 21P amplifier is operated, i.e., the transistor 217 is turned ON to increase the forward current I, so that the voltage VCOM slowly recovers its original level VIN with a time $\tau 1'$. In this case, an overshoot may be generated; however, no substantial overshoot as indicated in X1' is generated due to the presence of the offset voltage.

Thus, in the LCD driving apparatus of Fig. 20, discharging amplifier forming one push-pull type amplifier is of a rapid type, the transient response as shown in Fig. 24 is rapid which would invite no flicker.

In Fig. 19, when the offset voltage ΔV is decreased, the transient response speed can be increased as shown in Fig. 25. In this case, however, since the turning-ON period T_d of the discharging transistor 207 of Fig. 16 is superimposed onto the turning-ON period T_c of the charging transistor 217 of Fig. 16, an ON-ON current may flow therethrough during a period Δ

T. Similarly, since the turning-ON period T_c' of the charging transistor 217 of Fig. 16 is superimposed onto the turning-ON period T_d' of the discharging transistor 207 of Fig. 16, an ON-ON current may flow therethrough during a period ΔT'.

5   In Fig. 26, which illustrates a third embodiment of the LCD driving apparatus according to the present invention, the gradation voltage generating circuit 1 of Fig. 15 is replaced by a gradation voltage generating circuit 3.

In the gradation voltage generating circuit 3, 10   resistors r1', r2', r3' and r4' for other offset voltages are inserted in series with the resistors R1, R2, R3 and R4 of Fig. 15. Also, the push-pull type amplifiers 11, 12, 13 and 14 of Fig. 15 are replaced by push-pull type amplifiers 31, 32, 33 and 34, respectively. Each of the push-pull type amplifiers 15   31, 32, 33 and 34 further includes a rapid discharging amplifier such as 11n in addition to the slow discharging amplifier such as 11N and the rapid charging amplifier 11p as illustrated in Fig. 27.

In Fig. 27, the rapid discharging amplifier such as 20   11n has the same configuration as the slow discharging amplifier 11N except that the capacitor 208 is not provided.

The operation of the push-pull type amplifier of Fig. 27 will be explained next with reference to Figs. 28 and 29. In Fig. 28, the push-pull type amplifier of Fig. 27 is 25   connected by the decoder 102 to the liquid crystal panel 104 so that the voltage VCOM at the common electrode COM is VCOM = VIN while the voltage VSEG at the segment electrode SEG receives a voltage VL or VH via the decoder 103. In this case, the voltage (VCOM - VIN)-to-current I characteristics of the 30   push-pull type amplifier of Fig. 28 are shown in Fig. 29. In Fig. 29, if VCOM > VIN, the current I is very large due to the turning-ON of the transistors 207 and 207' of Fig. 27. Also, if $0 < VCOM - VIN \leqq \Delta V$, the current I is relatively large

due to the turning-ON of the transistor 207 of Fig. 27. On the other hand, if VCOM < VIN - ΔV, the current I is very large due to the turning-ON of the transistor 217.

Note that the rapid amplifiers 11p and 11n may

5 easily oscillate; in this case, however, since the rapid amplifiers 11p and 11n connected to the slow discharging amplifier 11N which may hardly oscillate, the rapid amplifiers 11p and 11n hardly oscillate.

Next, the transient characteristics of the voltage

10 VCOM of Fig. 28 are explained with reference to Fig. 30.

First, at time t1, when the voltage VSEG is increased by the decoder 103 from VL to VH, the voltage VCOM is also increased by the capacitive coupling. In this case, the rapid discharging amplifier 11n and the slow discharging

15 amplifier 11N are operated, i.e., the transistors 207 and 207' are turned ON to increase the backward current I, so that the voltage VCOM very rapidly recovers its original level VIN with a time τ0. In this case, an undershoot as indicated by X0 is generated, however, afterward, the operation of the rapid

20 discharging amplifier 11n is stopped, i.e., only the slow discharging amplifier 11N is operated. As a result, the undershoot as indicated by X0 is relatively small, so that the response speed is increased.

Next, at time t2, when the voltage VSEG is decreased

25 by the decoder 103 from VH to VL, the voltage VCOM is also decreased by the capacitive coupling. In this case, the rapid charging amplifier 11p is operated, i.e., the transistor 217 is turned ON to increase the forward current I, so that the voltage VCOM rapidly recovers its original level VIN with a

30 time τ0'. In this case, a large overshoot may be generated; however, no substantial overshoot as indicated by X0' is generated due to the presence of the offset voltage ΔV.

Thus, in the LCD driving apparatus of Fig. 26, the

discharging amplifiers and the charging amplifier forming one push-pull type amplifier are substantially of a rapid type, even if the offset voltage ΔV is large, the transient response as shown in Fig. 30 is rapid which would invite no flicker.

5   In Fig. 24, when the offset voltage ΔV is decreased, the transient response speed can be increased as shown in Fig. 31. In this case, however, since the turning-ON period T_d of the discharging transistor 207 of Fig. 21 is superimposed onto the turning-ON period T_c of the charging transistor 217 of Fig.

10   16, an ON-ON current may flow therethrough during a period ΔT. Similarly, since the turning-ON period T_c' of the charging transistor 217 of Fig. 21 is superimposed onto the turning-ON period T_d' of the discharging transistor 207 of Fig. 21, an ON-ON current may flow therethrough during a period $\Delta T'$.

15   In Fig. 32, which illustrates a fourth embodiment of the LCD driving apparatus according to the present invention, the gradation voltage generating circuit 2 of Fig. 20 is replaced by a gradation voltage generating circuit 4.

In the gradation voltage generating circuit 4,

20   resistors r1', r2', r3' and r4' for other offset voltages are inserted in series with the resistors R1, R2, R3 and R4 of Fig. 20. Also, the push-pull type amplifiers 21, 22, 23 and 24 of Fig. 20 are replaced by push-pull type amplifiers 41, 42, 43 and 44, respectively. Each of the push-pull type amplifiers

25   41, 42, 43 and 44 further includes a rapid charging amplifier such as 21p in addition to the rapid discharging amplifier such as 21n and the slow charging amplifier 21p as illustrated in Fig. 33.

In Fig. 33, the rapid charging amplifier such as 21p

30   has the same configuration as the slow discharging amplifier 21N except that the capacitor 218 is not provided.

The operation of the push-pull type amplifier of Fig. 33 will be explained next with reference to Figs. 34 and 35.

In Fig. 34, the push-pull type amplifier of Fig. 27 is connected by the decoder 102 to the liquid crystal panel 104 so that the voltage VCOM at the common electrode COM is VCOM = VIN while the voltage VSEG at the segment electrode SEG

5 receives a voltage VL or VH via the decoder 103. In this case, the voltage (VCOM - VIN)-to-current I characteristics of the push-pull type amplifier of Fig. 34 are shown in Fig. 35. In Fig. 35, if VCOM > VIN, the current I is very large due to the turning-ON of the transistor 207 of Fig. 33. On the other hand,

10 if $-\Delta V$ < VCOM - VIN $\leq$ 0, the current I is relatively large due to the turning-ON of the transistor 217 of Fig. 33. Further, if VCOM $\leq$ VIN - ΔV, the current I is very large due to the turning-ON of the transistors 217 and 217' of Fig. 33.

Note that the rapid amplifiers 21p and 21n may

15 easily oscillate; in this case, however, since the rapid amplifiers 21p and 21n connected to the slow charging amplifier 21P which may hardly oscillate, the rapid amplifiers 21p and 21n hardly oscillate.

Next, the transient characteristics of the voltage

20 VCOM of Fig. 34 are explained with reference to Fig. 36.

First, at time t1, when the voltage VSEG is increased by the decoder 103 from VL to VH, the voltage VCOM is also increased by the capacitive coupling. In this case, the rapid discharging amplifier 21n is operated, i.e., the

25 transistor 207 is turned ON to increase the backward current I, so that the voltage VCOM very rapidly recovers its original level VIN with a time $\tau 0$. In this case, an undershoot as indicated X0 is generated.

Next, at time t2, when the voltage VSEG is decreased

30 by the decoder 103 from VH to VL, the voltage VCOM is also decreased by the capacitive coupling. In this case, the rapid charging amplifier 21p and the slow charging amplifier 21p are operated, i.e., the transistors 217 and 217' are turned ON

to increase the forward current I, so that the voltage VCOM very rapidly recovers its original level VIN with a time τ 0'. In this case, a large overshoot may be generated; however, no substantial overshoot as indicated by X0' is generated, because afterward, the operation of the rapid charging amplifier 21p is stopped, i.e., only the slow changing amplifier 21P is operated.

Thus, in the LCD driving apparatus of Fig. 32, the discharging amplifier and the charging amplifiers forming one push-pull type amplifier are substantially of a rapid type, even if the offset voltage Δ V is large, the transient response as shown in Fig. 36 is rapid which would invite no flicker.

In Fig. 37, which illustrates a modification of the push-pull amplifier of Fig. 27, the rapid discharging amplifier 11n and the slow discharging amplifier 11N of Fig. 27 are combined into one discharging amplifier 11 (n, N). That is, three operational amplifiers are provided in Fig. 27, while two operational amplifiers are provided in Fig. 37. As a result, the push-pull amplifier of Fig. 37 is smaller in size than that of Fig. 27.

In Fig. 37, an N-channel MOS transistor 371 and switches 372 and 373 are added to the slow discharging amplifier 11N of Fig. 27, thus realizing the discharging amplifier 11(n, N). When CNT = "0"(low), the switches 372 and 373 are turned ON and OFF, respectively, so that the transistor 371 is turned OFF and the capacitor 208 is active, and thus, the discharging amplifier 11(n, N) serves as the rapid discharging amplifier 11n of Fig. 27. On the other hand, when CNT = "1"(low), the switches 372 and 373 are turned OFF and ON, respectively, so that the transistor 371 is turned ON and the capacitor 208 is inactive, and thus, the discharging amplifier 11(n, N) serves as the slow discharging amplifier 11N of Fig. 27. In this case, the turning-ON transistor 371

serves as an offset voltage generator, and therefore, the resistors r1', r2', r3' and r4' of Fig. 26 are unnecessary.

In Fig. 38, which illustrates a modification of the push-pull amplifier of Fig. 33, the rapid charging amplifier 21p and the slow charging amplifier 21P of Fig. 33 are combined into one charging amplifier 21 (p, P). That is, three operational amplifiers are provided in Fig. 33, while two operational amplifiers are provided in Fig. 38. As a result, the push-pull amplifier of Fig. 38 is smaller in size than that of Fig. 33.

In Fig. 38, a P-channel MOS transistor 381 and switches 382 and 383 are added to the slow charging amplifier 21P of Fig. 33, thus realizing the charging amplifier 21(p, P). When CNT = "0"(low), the switches 382 and 383 are turned ON and OFF, respectively, so that the transistor 381 is turned OFF and the capacitor 218 is active, and thus, the charging amplifier 21(p, P) serves as the rapid charging amplifier 21p of Fig. 33. On the other hand, when CNT = "1"(low), the switches 382 and 383 are turned OFF and ON, respectively, so that the transistor 381 is turned ON and the capacitor 218 is inactive, and thus, the charging amplifier 21(p, P) serves as the slow charging amplifier 21P of Fig. 33. In this case, the turning-On transistor 381 serves as an offset voltage generator, and therefore, the resistors r1', r2', r3' and r4' of Fig. 32 are unnecessary.

The control signal CNT and its inverted signal of Figs. 37 and 38 are shown in Fig. 39. That is, when the data signal DT is changed, the control signal CNT and its inverted signal are changed for a predetermined time period, so that the discharging amplifier 11(n, N) of Fig. 37 or the charging amplifier 21(p, N) of Fig. 38 carries out a slow discharging or charging operation.

In Fig. 40, which illustrates a modification of the

push-pull amplifier of Fig. 28, switches 401, 402 and 403 controlled by control signals CNT1 and CNT2 are added to the push-pull amplifier of Fig. 28. That is, the three operational amplifiers are always activated in Fig. 28, while the

5   operational amplifiers are selected and activated in Fig. 40. As a result, the power consumption of the push-pull amplifier of Fig. 40 is smaller than that of the push-pull amplifier of Fig. 28.

In Fig. 40, when the control signal CNT1 and CNT2

10   are "0"(low) and "1"(high), respectively, the rapid amplifiers 11n and 11p are activated. On the other hand, when the control signals CNT1 and CNT2 are "1"(high) and "0"(low), respectively, the slow amplifier 11N is activated.

In Fig. 41, which illustrates a modification of the

15   push-pull amplifier of Fig. 34, switches 411, 412 and 413 controlled by control signals CNT1 and CNT2 are added to the push-pull amplifier of Fig. 34. That is, the three operational amplifiers are always activated in Fig. 34, while the operational amplifiers are selected and activated in Fig. 41.

20   As a result, the power consumption of the push-pull amplifier of Fig. 41 is smaller than that of the push-pull amplifier of Fig. 34.

In Fig. 41, when the control signals CNT1 and CNT2 are "0"(low) and "1"(high), respectively, the rapid amplifiers

25   21n and 21p are activated. On the other hand, when the control signals CNT1 and CNT2 are "1"(high) and "0"(low), respectively, the slow amplifier 21P is activated.

The control signals CNT1 and CNT2 of Figs. 40 and 41 are shown in Fig. 42. That is, when the data signal DT is

30   changed, the control signals CNT1 and CNT2 are changed for a predetermined time period, so that the amplifiers 11p and 11n of Fig. 40 or the rapid amplifiers 21p and 21n of Fig. 41 carry out a rapid discharging or charging operation.

The present invention can be applied to a voltage generating apparatus other than a gradation voltage generating circuit in an LCD apparatus.

As explained hereinabove, since at least one rapid
5 amplifier is included in a push-pull type amplifier of a voltage generating apparatus, the transient response characteristics can be rapid. Also, since a slow amplifier is included in the push-pull type amplifier, the rapid amplifier hardly oscillates.
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